Abstract

Automatic Layout of Analog and Digital Mixed Macro/Standard Cell Integrated Circuits

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This thesis presents computer algorithms for the design of electronic integrated circuits or microchips. As consumer demand increases for such circuits, IC manufacturers are continually faced with a dilemma; provide superior products in shorter time frames. Provided within are advantageous techniques to relieve this time-to-market crisis. Specifically, algorithms are presented to reduce the time of the physical design (layout) phase, the placement and interconnection of the transistors which constitute the integrated circuit.

TimberWolf version 7, a new fully automatic placement and routing system is described. This tool exploits the advantages of the semicustom design style through the combination of macro and standard cells. Additionally, we will present a simulated annealing macro cell layout program which features new methods for statistical wiring estimation, placement refinement, and detailed routing.

Performance and area are the fundamental objectives of layout tools. A novel algorithm which controls timing delay without the need for user path specification is presented. This algorithm was able to increase the speed of the *fract* benchmark chip by 34% at an area cost of only 2.5%.We will present the first generalized row-based global router suitable for standard cell, gate-array, sea-of-gates, and FPGAs that explicitly minimizes chip area. This new global router adapts to technologies enabling it to outperform its predecessors.