

# References

- [1] E. H. L. Aarts, F. M. J. de Bont, J. H. A. Habers, and P. J. M. van Laarhoven, "Parallel Implementation of the Statistical Cooling Algorithm," *Integration*, Vol 4. No. 3, 1986, pp. 209-238.
  - [2] S. K. Abd-El-Hafiz, V. R. Basili, and G. Caldiera, "Towards Automated Support for Extraction of Reusable Components," *Proc. IEEE Conference of Software Maintenance*, 1991, pp. 212-219.
  - [3] W. Allen, D. Rosenthan, and K. Fiduk, "The MCC CAD Framework Methodology Management System," *Proc. Design Automation Conference*, 1991, pp. 694-698.
  - [4] K. Aoshima and E. S. Kuh, "Multichannel Optimization in Gate Array LSI Layout," *Proc. ISCAS*, 1983, pp. 1005-1008.
  - [5] T. Asano, and S. Sato, "Long Path Enumeration Algorithms for Timing Verification on Large Digital Systems," in Graph Theory with Applications to Algorithms and Computer Sciences, Wiley and Sons, 1985, pp. 25-35.
  - [6] P. Banerjee and M. Jones, "A Parallel Simulated Annealing Algorithm for Standard Cell Placement on a Hypercube Computer," *Proc. of Intl. Conf. on Computer-Aided Design*, 1986, pp. 34-37.
  - [7] J. Benkoski and R. B. Stewart, "TATOO: An Industrial Timing Analyzer with False Path Elimination and Test Pattern Generation," *Proc. European Conf. on Design Automation*, 1991, pp. 256-260.
  - [8] J. Benkoski and A. Strojwas, "The Role of Timing Verification in Layout Synthesis," *Proc. Design Automation Conference*, June, 1991, pp. 612-619.
  - [9] J. Bentley, Writing Efficient Programs, (Englewood Cliffs : Pentice-Hall, 1982).
-

- [10] J. Bentley, Programming Pearls, (Reading : Addison-Wesley Publishing Company, 1982).
- [11] J. Bentley, Programming Pearls, (Reading: Addison-Wesley Publishing Company, 1988).
- [12] M. W. Bern, "Two Probabilistic Results on Rectilinear Steiner Trees," *Algorithmica* 3, 1988, pp. 191-204.
- [13] M. W. Bern and M. De Carvalho, "A Greedy Heuristic for the Rectilinear Steiner Tree Problem," *Report No UCB/CSD 87/306*, Computer Science Division, University of California, Berkeley, 1986.
- [14] J. Blair, S. Kapoor, E. Lloyd, and K. Supowit, "Minimizing Channel Density in Standard Cell Layout," *Algorithmica* 2 1987, pp. 267-282.
- [15] J. Blanks, "Near-optimal Placement using a Quadratic Objective Function," *Proc. 21st Design Automation Conference*, 1985, pp. 609-615.
- [16] M. A. Breuer, "Min-Cut Placement", *Journal of Design Automation and Fault Tolerant Computing*, Vol. 1, No. 4 , 1977, pp. 343-362.
- [17] R. Brouwer and P. Banerjee, "A Parallel Hierarchical Global Router," *IEEE Trans. on Computer-Aided Design*, Vol. CAD-2, No. 4, pp. 223-234.
- [18] T. Bull, "An Introduction to the WSL Program Transformer," *Proc. IEEE Conference on Software Maintenance*, 1990, pp. 242-250.
- [19] J. L. Burns and A. R. Newton, "SPARCS: A New Constraint-Based IC Symbolic Layout Spacer," *Proc. of CICC*, 1986, pp. 534-539.
- [20] J. Burns, A. Casotto, M. Igusa, F. Marron, F. Marron, F. Romeo, A. Sangiovanni-Vincentelli, C. Sechen, H. Shin, G. Srinath, and H. Yaghtiel, "Mosaico: An Integrated Macro-Cell Layout System," *Proc. of VLSI '87*, Vancouver, Canada, August, 1987.
-

- [21] M. Burstein and R. Pelavin, "Hierarchical Wire Routing," *IEEE Trans. Computer-Aided Design*, Vol. CAD-2, 1983, pp. 223-234.
- [22] M. Burstein, and R. Pelavin, "Hierarchical Channel Router", *Proc. 20th Design Automation Conference*, June 1983, pp. 591-597.
- [23] M. Burstein and M. N. Youseff, "Timing Influenced Layout Design," *Proc. 22th Design Automation Conference*, 1985, pp. 124-130.
- [24] R. C. Carden and C. Cheng, "A Global Router Using an Efficient Approximate Multicommodity Multiterminal Flow Algorithm," *Proc. Design Automation Conference*, 1991, pp. 316-321.
- [25] R. Carey and M. Bendick, "The Control of a Software Test Process," *Proc. IEEE Conference on Computer Software and Applications*, 1977, pp. 327-334.
- [26] A. Casotto, F. Romeo, and A. Sangiovanni-Vincentelli, "A Parallel Simulated Annealing Algorithm for the Placement of Macro-Cells." *IEEE Trans. on Computer-Aided Design of ICs and Systems*, Vol. 6, No. 5, 1987, pp. 838-847.
- [27] A. Casotto, A. R. Newton, and A. Sangiovanni-Vincentelli, "Design Management Based on Design Traces," *Proc. Design Automation Conference*, 1990, pp. 136-141.
- [28] E. Charbon, E. Malavasi, U. Choudhury, A. Casotto, and A. Sangiovanni-Vincentelli, "A Constraint-Driven Placement Methodology for Analog Integrated Circuits," *Proc. of Custom Integrated Circuits Conference*, 1992, pp. 28.2.1-28.2.4.
- [29] D. Chen and C. Sechen, "Mickey: A Macro Cell Global Router," *Proc. European Conf. on Design Automation*, 1991, pp. 248-252.
- [30] C. K. Cheng and E. S. Kuh, "Module Placement Based on Resistive Network Optimization," *IEEE Trans. Computer-Aided Design*, vol. CAD-3, July 1984, pp. 218-225.
-

- [31] M. Chi, "An Automatic Rectilinear Partitioning Procedure for Standard Cell." *Proc. 24th Design Automation Conference*, 1987, pp. 50-55.
- [32] S. Chopra and E. Rosenberg, "Efficient Method for Custom Integrated Circuit Global Routing", *Proc. IEEE Custom Integrated Circuits Conference*, May 1988, paper 11.3.
- [33] S. Chowdhury, "Optimum Design of Reliable IC Power Networks Having General Graph Topologies," *Proc. 26th Design Automation Conference*, June 1989, pp.787-790.
- [34] J. K. Chua and Y. C. Lim, "Fast Vicinity-Upgrade Algorithm for Rectilinear Steiner Trees," *Electronic Letters*, Vol 27. No. 13, June 1991, pp. 1139-1140.
- [35] J. M. Cohn, D. J. Garrod, R. Rutenbar, and L. R. Carley, "KOAN/ANAGRAM II: New Tools for Device-Level Analog Placement and Routing," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 3, March 1991, pp. 330-342.
- [36] J. M. Cohn, D. J. Garrod, R. Rutenbar, and L. R. Carley, "Technique for Simultaneous Placement and Routing of Custom Analog Cells in KOAN/ANAGRAM II," *Proc. of IEEE Intl Conf. on Computer-Aided Design*, 1991, pp 394-397.
- [37] J. P. Cohoon, S. U. Hegde, W. N. Martin, and D. Richards, "Floorplan Design using Distributed Genetic Algorithms," *Proc. IEEE Intl. Conf. on Computer-Aided Design*, 1988, pp. 452-455.
- [38] J. P. Cohoon and P. L. Heck, "BEAVER: A Computational-Geometry-Based Tool for Switchbox Routing," *IEEE Trans. on CAD*, Vol. 7, No. 6, pp. 684-697.
- [39] R. Condamoor and I. G. Tollis, "A New Heuristic for Rectilinear Steiner Trees," *Proc. IEEE Intl. Symposium on Circuits and Systems*, 1990, pp. 1676-1677.
- [40] J. Cong and B. Preas, "A New Algorithm for Standard Cell Global Routing," *Proc. IEEE Intl. Conf. on Computer-Aided Design*, 1988, pp. 176-179.
-

- [41] J. Cong, A. Kahng, G. Robins, M. Sarrafzadeh, and C. K. Wong, "Provably Good Performance-Driven Global Routing," *IEEE Trans. on Computer-Aided Design*, Vol. 11, No. 6, 1992, pp. 739-751.
- [42] T. H. Cormen, C. E. Leiserson, and R. L. Rivest, Introduction to Algorithms, (Cambridge: The MIT Press, 1990), pp. 23-41.
- [43] T. H. Cormen, C. E. Leiserson, and R. L. Rivest, Introduction to Algorithms, (Cambridge: The MIT Press, 1990), p. 87.
- [44] T. H. Cormen, C. E. Leiserson, and R. L. Rivest, Introduction to Algorithms, (Cambridge: The MIT Press, 1990), p. 329-355.
- [45] T. H. Cormen, C. E. Leiserson, and R. L. Rivest, Introduction to Algorithms, (Cambridge: The MIT Press, 1990), p. 463-497.
- [46] T. H. Cormen, C. E. Leiserson, and R. L. Rivest, Introduction to Algorithms, (Cambridge: The MIT Press, 1990), p. 932.
- [47] W. Dai, H. Chen, R. Dutti, M. Jackson, E. Kuh, M. Marek-Sadowska, M. Sato, D. Wang, and X. Xiong, "BEAR: A New Building-Block Layout System," *Proc. Int. Conf. on Computed-Aided Design*, 1987, pp. 34-37.
- [48] D. N. Deutsch, "A Dogleg Channel Router", *Proc. 13th Design Automation Conference*, June 1976, pp. 425-433.
- [49] R. Dietz, D. A. Mlynski, "New Model for Global Routing of Gate-Arrays," *Proc. IEEE International Symposium on Circuits and Systems*, May 1987, pp. 35-38.
- [50] E. W. Dijkstra, "A Note on Two Problems in Connexion with Graphs," *Numerische Mathematik*, Vol. 1, 1959, pp. 269-271.
- [51] E. W. Dijkstra, "Go To Statement Considered Harmful," *Communications of the ACM*, Vol. 11, No. 3, 1968, pp. 147-148.
-

- [52] E. W. Dijkstra, "A Constructive Approach to the Problem of Program Correctness," *BIT*, Vol. 8, No. 3, 1968, pp. 174-186.
- [53] W. Donath, R. Norman, B. Agrawal, S. Bello, S. Han, J. Kurtzberg, P. Lowy, and R. McMillan, "Timing Driven Placement using Complete Path Delays," *Proc. Design Automation Conference*, June 1990, pp. 84-89.
- [54] S. E. Dreyfus, "An Appraisal of Some Shortest-Path Algorithms," *Operations Research*, Vol. 17, 1969, pp. 395-412.
- [55] A. E. Dunlop, V. D. Agrawal, D. N. Deutsch, M. F. Jukl, P. Kozak, and M. Wiesel, "Chip Layout Optimization Using Critical Path Weighting," *Proc. 21st Design Automation Conference*, 1984, pp. 133-136.
- [56] A. E. Dunlop and B. Kernighan, "A Procedure for Placement of Standard-Cell VLSI Circuits," *IEEE Trans. on Computer-Aided Design*, Vol. 4, No. 1, 1985, pp. 92-98.
- [57] A. E. Dunlop, G. F. Gross, C. D. Kimble, M. Y. Luong, K. J. Stern, and E. J. Swanson, "Features in LTX2 for Analog Layout," *Proc. of ISCAS*, 1985, pp. 21-23.
- [58] R. Dutta and M. Marek-Sadowska, "Automatic Sizing of Power/Ground (P/G) Networks in VLSI," *Proc. 26th Design Automation Conference*, June 1989, pp.783-786.
- [59] C. Ebeling and O. Zajicek, "Validating VLSI Circuit Layout by Wirelist Comparison," *Digest Intl. Conf. on Computer-Aided Design*, 1983, pp.172-173
- [60] M. Edahiro, T. Yoshimura, "New Placement and Global Routing Algorithms for Standard Cell Layouts," *Proc. Design Automation Conference*, 1990, pp. 642-645.
- [61] S. Even, Graph Algorithms, (Potamac: Computer Science Press, 1979), pp. 138-142.
- [62] R. J. Evans, "SMARTsystem: A CASE Development Environment for Existing C Programs," *Proc. IEEE Conference on Software Maintenance*, 1990, p. 256.
-

- [63] P. de Forcrand and H. Zimmermann, "Timing-Driven Auto-Placement," *Proc. Int. Conf on Comp. Design*, 1987, pp. 518-521.
- [64] C. Fiduccia and R. Mattheyses, "A Linear Time Heuristic for Improving Network Partitions," *Proc. 19th Design Automation Conference*, 1982, pp. 175,181.
- [65] R. Fiebrich and C. Wang, "Circuit Placement Based on Simulated Annealing on a Massively Parallel Computer," *Proc. Intl. Conf. on Computer Design*, 1987, pp. 78-82.
- [66] L. R. Ford and D. R. Fulkerson, Flows in Networks, (Princeton: Princeton University Press, 1962).
- [67] J. Frankle and R. Karp, "Circuit Placements and Cost Bounds by Eigenvector Decomposition," *Digest Intl. Conference on Computer-Aided Design*, 1986, pp. 414-417.
- [68] K. Fukahori, "Computer Simulation of Integrated Circuits in the Presence of Electrothermal Interaction," *IEEE Journal of Solid-state Circuits*, Vol. 11, No. 6, 1976.
- [69] K. Fukunaga, S. Yamada, H. Stone, and T. Kasai, "Placement of Circuit Modules Using a Graph Space Approach," *Proc. 20th Design Automation Conference*, 1983, pp. 465-471.
- [70] J. D. Gannon, R. G. Hamlet, and H. D. Mills, "Theory of Modules," *IEEE Trans. on Software Engineering*, Vol. SE-13, No. 7, July 1987, pp. 820-829.
- [71] T. Gao, P. M. Vidya, and C. L. Liu, "A New Performance Driven Placement Algorithm," *Proc. ICCAD*, November 1991, pp. 44-47.
- [72] T. Gao, P. M. Vidya, and C. L. Liu, "A Performance Driven Macro-Cell Placement Algorithm," *Proc. Design Automation Conference*, June 1992, pp. 147-152.
-

- [73] M. R. Garay and D. S. Johnson, Computers and Intractability: A Guide to the Theory of NP-Completeness, (New York: W. H. Freeman and Company, 1979).
- [74] D. Garrod, R. Rutenbar, L. Carley, "Automatic Layout of Custom Analog Cells in ANAGRAM," *Proc. of ICCAD*, 1988, pp. 544-547.
- [75] V. R. Gibson and J. A. Senn, "System Structure and Software Maintenance Performance," *CACM*, Vol. 32, No. 3, 1989, pp. 347-358.
- [76] S. Goto and E. Kuh, "An Approach to the Two-Dimensional Placement Problem in Circuit Layout," *IEEE Trans. on Circuits and Systems*, Vol. 25, No. 4, 1978, p. 208.
- [77] S. Goto and T. Matsuda, "Partitioning, Assignment and Placement," in Layout Design and Verification, edited by T. Ohtsuki, (Amsterdam: North Holland, 1986), pp. 76-82.
- [78] P. Groeneveld, "On Global Wire Ordering for Macro-Cell Routing." *Proc. 26th Design Automation Conference*, 1989, pp. 155-160.
- [79] K. Hall, "An r-Dimensional Quadratic Placement Algorithm, *Management Science*, Vol. 17. No. 3, 1970, pp. 219-229.
- [80] G. T. Hamachi and J. K. Ousterhout, "A Switchbox Router with Obstacle Avoidance," *Proc. Design Automation Conference*, 1984, pp. 173-179.
- [81] T. Hamada, C. Cheng, and P. Chau, "A Wire Length Estimation Technique Utilizing Neighborhood Density Equations," *Proc. Design Automation Conference*, 1992, pp. 57-61.
- [82] M. Hanan, "On Steiner's Problem With Rectilinear Distance", *SIAM J. of Applied Mathematics*, Vol. 14, 1966, pp. 255-265.
- [83] M. Hanan and J. Kurtzberg, Design Automation of Digital Systems : Theory and Techniques, edited by M. Breuer, (Englewood Cliffs: Prentice-Hall, Inc., 1972), pp. 214-224.
-

- [84] N. Hasan, G. Vijayan, and C. K. Wong, "A Neighborhood Improvement Algorithm for Rectilinear Steiner Trees," *Proc. IEEE Intl Symp. on Circuits and Systems*, 1990.
- [85] T. Hasegawa, "A New Placement Algorithm Minimizing Path Delays," *Proc. ICCAD*, 1991, pp. 2052-2055.
- [86] A. Hashimoto and J. Stevens, "Wire Routing by Optimizing Channel Assignment within Large Apertures", *Proc. 8th Design Automation Workshop*, 1971, pp. 155-163.
- [87] G. D. Hachtel and C. R. Morrison, "Linear Complexity Algorithms for Hierarchical Routing," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* Vol. 8, No. 1, Jan 1989, pp. 64-80.
- [88] P. Hauge, R. Nair, and E. Yoffa, "Circuit Placement for Predictable Performance." *Proc. Intl. Conf. on Computed-Aided Design*, 1987, pp. 88-91.
- [89] D. W. Hightower, "A Solution to the Line Routing Problem on a Continuous Plane", *Proc. 6th Design Automation Workshop*, 1969 pp. 1-24.
- [90] H. Hillner, B. Weis, D. Mlynski, "The Discrete Placement Problem: a Dynamic Programming Approach," *Proc. Intl. Symposium on Circuits and Systems*, 1986, pp. 315-318.
- [91] R. B. Hitchcock, G. L. Smith, D. D. Cheng, "Timing analysis of computer hardware," *IBM Journal of Research and Development*, Vol 24, No. 1, Jan. 1983, pp. 100-105.
- [92] J. M. Ho, G. Vijayan and C. K. Wong, "New Algorithms for the Rectilinear STEiner Tree Problem", *IEEE Trans. on Computer-Aided Design*, Vol 9-2, 1990, pp. 185-193.
- [93] C. A. R. Hoare, "Proof of Correctness of Data Representations," *Acta Inform.*, Vol. 1, 1972, pp. 271-281.
- [94] M. Horowitz and R. W. Dutton, "Resistance Extraction from Mask Layout Data," *IEEE Trans. on Computer-Aided Design*, Vol. 2. No. 3, July 1983, pp. 145-150.
-

- [95] F. K. Hwang, "On Steiner Minimal Trees with Rectilinear Distance," *SIAM J. Applied Mathematics*, Vol. 30(1), 1976, pp. 104-114.
- [96] F. K. Hwang, "An  $O(n \log n)$  Algorithm for Suboptimal Rectilinear Steiner Trees," *J. ACM*, Vol. 26-2, 1979, pp. 177-182.
- [97] M. Igusa, M. Beardslee, A. Sangiovanni-Vincentelli, "ORCA: A sea-of-gates place and route system", *Proc. Design Automation Conference*, June 1989, pp. 122-127.
- [98] M. Jackson and E. Kuh, "Performance-Driven Placement of Cell Based IC's," *Proc. Design Automation Conference*, June 1989, pp. 370-375.
- [99] M. Jackson, E. Kuh, and M. Marek-Sadowska, "Timing-Driven Routing for Building Block Layout," *Proc. of ISCAS*, 1987, pp. 518-519.
- [100] M. Jackson, A. Srinivasan, and E. Kuh, "A Fast Algorithm for Performance-Driven Placement," *Proc. Int. Conf. on Computer-Aided Design*, 1990, pp. 328-331.
- [101] D. Jepsen and C. Gelatt, Jr., "Macro Placement by Monte Carlo Annealing." *Proc. Intl. Conf. on Comp. Design*, 1983, pp. 495-498.
- [102] R. Joobbani and D. Siewiorek, "WEAVER: A Knowledge-Based Routing Expert," *IEEE Design and Test of Computers*, Vol. 3. No. 1, Feb. 1986, pp. 12-23.
- [103] A. Kahng and G. Robins, "On Performance Bounds for a Class of Rectilinear Steiner Tree Heuristics in Arbitrary Dimension", *IEEE Trans. on Computer-Aided Design*, Vol. 11, No. 11, 1992, pp. 1462-1465.
- [104] A. Kahng and G. Robins, "A New Class of Iterative Steiner Tree Heuristics with Good Performance", *IEEE Trans. on Computer-Aided Design*, Vol. 11, No. 7, pp. 893-902.
- [105] R. M. Karp, "Reducibility Among Combinatorial Problems," *Complexity of Computer Computations*, New York: Plenum, 1972.
-

- [106] Y. Kashai, "Flow - A Concurrent Methodology Manager," *European Conference on Design Automation*, 1992, pp. 20-24.
- [107] D. Keller, "A Guide to Natural Naming," *SIGPLAN Notices*, Vol. 25, No. 5, pp. 95-102.
- [108] B. W. Kernighan and S. Lin, "An Efficient Heuristic Procedure for Partitioning Graphs," *Bell Syst. Tech. J.*, Vol. 49, No. 2, Feb. 1970, pp. 219-307.
- [109] B. W. Kernighan and D. M. Ritchie, The C Programming Language, (Englewood Cliffs: Prentice Hall, 1988).
- [110] K. Keutzer, S. Malik, and A. Saldanha, "Is Redundancy Necessary to Reduce Delay?," *IEEE Trans. on CAD*, CAD-10 No. 4, April 1991, pp. 427-435.
- [111] C. D. Kimble, A. E. Dunlop, G. F. Gross, V. L. Hein, M. Y. Luong, K. J. Stern, and E. J. Swanson, "Autorouted Analog VLSI," *Proc. Custom Integrated Circuits Conference*, 1985, pp. 72-78.
- [112] S. Kirkpatrick, C. D. Gelatt, Jr., and M. P. Vecchi, "Optimization by Simulated Annealing," *Science*, Vol. 220, May 1983, pp. 671-680.
- [113] J. Kleinhans, G. Sigl, and F. Johannes, "Gordian: A New Global Optimization / Rectangle Dissection Method for Cell Placement," *Proc. ICCAD*, 1988, pp. 506-509.
- [114] R. Kling and P. Banerjee, "ESP: A New Standard Cell Placement Package Using Simulated Evolution," *Proc. Design Automation Conference*, June 1987, pp. 60-66.
- [115] R. Kling and P. Banerjee, "ESP: Placement by Simulated Evolution," *IEEE Trans. on Computer-Aided Design*, Vol. 7, No. 3, March 1989, pp. 245-256.
- [116] R. Kling and P. Banerjee, "Empirical and Theoretical Studies of the Simulated Evolution Method Applied to Standard Cell Placement," *IEEE Trans. on Computer-Aided Design*, Vol. 10, No. 10, October 1991, pp. 1303-1315.
-

- [117]D. E. Knuth, The Art of Computer Programming, Volume I, Fundamental Algorithms, (Reading: Addison-Wesley, 1968).
- [118]D. E. Knuth, "Structure Programming with GO TO Statements," *Computing Surveys*, Vol. 6, No. 4, 1974, pp. 261-301.
- [119]D. E. Knuth, Literate Programming, (Leland: Center for the Study of Language and Information, 1992), pp. 99-358.
- [120]H. Koh, C. Sequin, and P. Gray, "Automatic Synthesis of Operational Amplifiers Based on Analytic Circuit Models," *Proc. ICCAD*, 1987, pp. 502-505.
- [121]H. Koh, C. Sequin, and P. Gray, "Automatic Layout Generation for CMOS Operational Amplifiers," *Proc. ICCAD*, 1988, pp. 548-551.
- [122]S. A. Kravitz and R. R. Rutenbar, "Placement by Simulated Annealing on a Multiprocessor," *IEEE Trans. on Computer-Aided Design*, CAD-6, No. 4, pp. 534-549, 1987.
- [123]J. Lam and J. M. Delosme, "An Efficient Simulated Annealing Schedule: Derivation", *Yale University Technical Report 8816*, Department of Electrical Engineering, Yale University, New Haven, CT, 1988.
- [124]J. Lam and J. M. Delosme, "An Efficient Simulated Annealing Schedule: Implementation and Evaluation", *Yale University Technical Report 8817*, Department of Electrical Engineering, Yale University, New Haven, CT, 1988.
- [125]J. Lam and J. M. Delosme, "An Efficient Simulated Annealing Schedule." *Yale University Technical Report 8818*, Department of Electrical Engineering, New Haven, CT, 1988.
- [126]J. Lam and J. M. Delosme, "Performance of a New Annealing Schedule." *Proc. 25th Design Automation Conf.*, 1988, pp. 306-311.
-

- [127]U. Lauther, "A Min-Cut Placement Algorithm for General Cell Assemblies Based on a Graph Representation," *Proc. 16th Design Automation Conference*, 1979, pp. 1-10.
- [128]E. Lawler, Combinatorial Optimization: Networks and Matroids, (New York: Holt, Rinehart, and Winston, 1976), pp. 98-106.
- [129]C. Lee, "An Algorithm for Path Connections and its Applications", *IRE Trans. on Electronic Computers*, VEC-10, Sept. 1961, pp. 346-365.
- [130]K. W. Lee, "Global Routing of Row-Based Integrated Circuits," Ph.D. thesis Yale University, May 1990, p. 109.
- [131]K. W. Lee and C. Sechen, "A New Global Router for Row-Based Layout," *Proc. IEEE Intl. Conf. on Computer-Aided Design*, 1988, pp. 180-183.
- [132]K. W. Lee and C. Sechen, "A Global Router for Sea-of-Gates Circuits," *Proc. European Conf. on Design Automation*, 1991, pp. 242-247.
- [133]J. H. Lee, N. K. Bose and F. K. Hwang, "Use of Steiner's Problem in Sub-Optimal Routing in Rectilinear Metric," *IEEE Trans. on Circuits and Systems*, CAS-23, 1976, pp. 470-476.
- [134]T. Lengauer, Combinatorial Algorithms for Integrated Circuit Layout, (Chichester: John Wiley & Sons, 1990), pp. 31-45.
- [135]S. Letovsky and E. Soloway, "Delocalized Plans and Program Comprehension," *IEEE Software*, May 1986, pp. 41-49.
- [136]H. Leung and L. White, "A Study of Integration Testing and Software Regression at the Integration Level," *Proc. IEEE Conference on Software Maintenance*, 1990, pp. 290-301.
- [137]Y. Z. Liao and C. K. Wong, "An Algorithm to Compact a VLSI Symbolic Layout with Mixed Constraints," *IEEE Trans. on Computer-Aided Design of Integrated Circuits*, Vol. 2, No. 2, pp. 62-69, 1983.
-

- [138]J. T. Li and M. Marek-Sadowska, "Global Routing for Gate Arrays," *IEEE Trans. on Computer-Aided Design*, Vol. 3, No. 4, October, 1984, pp. 298-307.
- [139]R. Libeskind-Hadas and C. L. Liu, "Solutions to the Module Orientation and Rotation Problems by Neural Computation Networks," *Proc. Design Automation Conference*, 1989, pp. 400-405.
- [140]R. Lin and E. Shragowitz, "Fuzzy Logic Approach to Placement Problem," *Proc. Design Automation Conference*, 1992, pp. 153-158.
- [141]B. W. Lindsay and B. T. Preas, "Design Rule Checking and Analysis of IC Mask Designs," *Proc. 13th Design Automation Conference*, 1976, pp. 301-308.
- [142]M. Lorenzetti, "The Effect of Channel Router Algorithms on Chip Yield", paper 4.2 Vol. 1, *Proc. International Workshop on Layout Synthesis*, May 8-11, 1990, MCNC Research Triangle Park, N.C.
- [143]W. Luk, "A Fast Physical Constraint Generator for Timing Driven Layout," *Proc. Design Automation Conference*, June 1991, pp. 626-631.
- [144]M. Marek-Sadowska, "Global Router for Gate Array," *Proc. IEEE Int. Conf. on Computer Design*, 1984, pp. 332-337.
- [145]M. Marek-Sadowska and S. Lin, "Timing Driven Placement." *Proc. Int. Conf. on Computed-Aided Design*, 1989, pp. 94-97.
- [146]S. Mayrhofer and U. Lauther, "Congestion-Driven Placement Using a New Multi-Partitioning Heuristic," *Proc. Int. Conf. on Computed-Aided Design*, 1990, pp. 332-335.
- [147]P. C. McGeer and R. K. Brayton, "Efficient Algorithms for Computing the Longest Viable Path in a Combinatorial Network," *Proc. 26th Design Automation Conference*, 1989, pp. 561-567.
-

- [148]C. Mead and L. Conway, Introduction to VLSI Systems, (Reading: Addison-Wesley, 1980).
- [149]C. Mead and L. Conway, Introduction to VLSI Systems, (Reading: Addison-Wesley, 1980), p. 52.
- [150]G. Meixner and U. Lauther, "A New Global Router Based on a Flow Model and Linear Assignment," *Proc. International Conference on Computer-Aided Design*, 1990, pp. 44-47.
- [151]N. Metropolis, A. Rosenbluth, and M. Rosenbluth, A. Teller, and E. Teller, *Journal of Chemical Physics*, Vol. 21, 1953, p. 1087.
- [152]K. Mikami and K. Tabuchi, "A Computer Program for Optimal Routing of Printed Circuit Connectors," *IFIPS Proc.*, Vol H47 pp. 1475-1478.
- [153]D. Mitra, R. Romeo, and A. Sangiovanni-Vincentelli, "Convergence and Finite-Time Behavior of Simulated Annealing," *Advances in Applied Probability*, Vol. 18. No. 3, pp. 747-771, 1986.
- [154]D. A. Mlynski and C. Sung, Layout Design and Verification, T. Ohtsuki, editor, (Amsterdam: Elsevier Science Publishers B. V., 1986), pp. 219.
- [155]M. Mogaki, C. Miura, and H. Terai, "Algorithm for Block Placement with Size Optimization Technique by the Linear Programming Approach," *Proc. Design Automation Conference*, 1987, pp. 80-83.
- [156]E. F. Moore, "The Shortest Path through a Maze," *Annals of the Harvard Computation Laboratory*, Vol. 30, Pt. II, 1959, pp. 185-292.
- [157]J. T. Mowchenko, C. S. Ma, "New Global Routing Algorithm for Standard Cell ICs," *Proc. Intl. Symposium on Circuits and Systems*, May 1987, pp. 27-30.
- [158]G. J. Myers, Software Reliability: Principles and Practices, (New York: Wiley-Interscience, 1976), p. 130.
-

- [159]G. J. Myers, Software Reliability: Principles and Practices, (New York: Wiley-Interscience, 1976), p. 169.
- [160]G. J. Myers, Software Reliability: Principles and Practices, (New York: Wiley-Interscience, 1976), p 190.
- [161]G. J. Myers, Software Reliability: Principles and Practices, (New York: Wiley-Interscience, 1976), pp. 169-195.
- [162]R. Nair, "A Simple Yet Effective Technique for Global Wiring," *IEEE Trans. Computer-Aided Design*, Vol. CAD-6, No. 2, March 1987, pp. 165-172.
- [163]A. Ng., P. Raghavan, and C. Thompson, "Experimental Results for a Linear Program Global Router," *Computers and Artificial Intelligence*, 1987.
- [164]T. Ohtsuki, editor, Layout Design and Verification, (North-Holland: Elsevier Science Publishers B. V., 1986), pp. 199-235.
- [165]H. Onodera, Y. Taniguchi, and K. Tamaru, "Branch-and-Bound Placement for Building Block Layout," *Proc. Design Automation Conference*, 1991, pp. 433-439.
- [166]J. K. Ousterhout, "Corner Stitching: A Data-Structure Technique for VLSI Layout Tools," *IEEE Trans. Computer-Aided Design*, Vol. CAD-3 pp. 87-100, Jan. 1984.
- [167]T. Parng and R. Tsay, "New Approach to Sea-of-gates Global Routing," *Proc. IEEE International Conference on Computer-Aided Design*, Nov. 1989, pp. 52-55.
- [168]M. Pedram and B. Preas, "Interconnection Length Estimation of Optimized Standard Cell Layouts," *Proc. Intl. Conf. on Computer-Aided Design*, Oct. 1989, pp. 100-108.
- [169]S. Prasitjutrakul and W. J. Kubitz, "A Timing-driven Global Router for Custom Chip Design", *Proc. Intl. Conf. on Computer-Aided Design*, 1990, pp. 48-51.
- [170]B.T. Preas, and M. J. Lorenzetti, editors, Physical Design Automation of VLSI Systems, (Menlo Park: The Benjamin/Cummings Publishing Company, Inc., 1988), p. 5.
-

- [171] B.T. Preas, and M. J. Lorenzetti, editors, Physical Design Automation of VLSI Systems, (Menlo Park: The Benjamin/Cummings Publishing Company, Inc., 1988), p. 264-265.
- [172] B.T. Preas, and M. J. Lorenzetti, editors, Physical Design Automation of VLSI Systems, (Menlo Park: The Benjamin/Cummings Publishing Company, Inc., 1988), pp. 347-407.
- [173] W. Press, B. Flannery, S. Teukolsky, and W. Vetterling, Numerical Recipes in C - The Art of Scientific Computing, (New York: Cambridge University Press, 1988), pp. 517-558.
- [174] R. Putatunda, D. Smith, M. Stebnisky, C. Puschak, and P. Patent, "VITAL: Fully Automatic Placement Strategies for Very Large Semicustom Designs." *Proc. IEEE International Conference on Computer Design: VLSI in Computers & Processors* 1988, pp. 434-439.
- [175] P. Raghavan, C. D. Thompson, "Multiterminal Global Routing: a Deterministic Approximation Scheme," *Algorithmica*, Vol. 6, No. 1, 1991, pp. 73-82.
- [176] K. Ramachandran, R. R. Cordell, D. F. Daly, D. N. Deutsch, and A. F. Kwan, "SYMCELL - A Symbolic Standard Cell System", *IEEE Journal of Solid State Circuits*, Vol. 26, No. 3, March 1991.
- [177] K. Ramachandran, D. G. Boyer, and R. R. Cordell, "SYMCELL II - A Second-Generation Symbolic Standard Cell System", *Proc. International Workshop on Layout Synthesis*, May 18-21, 1992. MCNC Research Triangle Park, N.C. , pp. 105-109.
- [178] C. P. RaviKumar and L.M. Patnaik, "Parallel Placement by Simulated Annealing," *Proc. Int. Conf on Comp. Design*, 1987. pp. 91-94.
-

- [179] J. Reed, A. Sangiovanni-Vincentelli, and M. Santomauro, "A New Symbolic Channel Router: YACR2", *IEEE Trans. on Computer-Aided Design*, Vol. CAD-4, No. 3, July 1985, pp. 208-219.
- [180] E. Reingold and K. Supowit, "Hierarchy-Driven Amalgamation of Standard and Macro Cells," *IEEE Trans. on CAD*, Vol. CAD-3, No. 1, Jan 1984, pp. 3-11.
- [181] D. Richards, "Fast Heuristic Algorithms for Rectilinear Steiner Trees," *Algorithmica* 4, 1989, pp. 191-207.
- [182] R. L. Rivest and C. M. Fiduccia, "A Greedy Channel Router," *Proc. 19th. Design Automation Conference*, June 1982, pp. 418-424.
- [183] K. Roberts, G. Fredericks, D. Skinner, D. Layman, and D. Harris, "Automatic Layout in the Highland System," *Proc. IEEE Intl. Conf on Computer-Aided Design*, 1984, pp. 224-226.
- [184] C. D. Rogers, J. B. Rosenberg, and S. W. Daniel, "MCNC's Vertically Integrated Symbolic Design System," *Proc. 22nd. Design Automation Conference*, June 1985, pp. 62-68.
- [185] J. Rose, "LocusRoute: A Parallel Global Router for Standard Cells," *Proc. Design Automation Conference*, 1988, pp. 189-195.
- [186] J. Rose and S. Brown, "Flexibility of Interconnection Structures for Field-Programmable Gate Arrays," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 3, March 1991, pp. 277-282.
- [187] J. Rose, R. Francis, D. Lewis, and P. Chow, "Architecture of Field-Programmable Gate Arrays: The Effect of Logic Block Functionality on Area Efficiency," *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 5, October 1990, pp. 1217-1225.
-

- [188]A. Saldanha, R. K. Brayton, and A. Sangiovanni-Vincentelli, "Circuit Structure Relations to Redundancy and Delay: the KMS Algorithm Revisted," *Proc. 29th Design Automation Conference*, 1992, pp. 245-248.
- [189]J. Sametiger, "A Tool for the Maintenance of C++ Programs," *Proc. IEEE Conference on Software Maintenance*, 1990, pp. 54-59.
- [190]S. Sahni and T. Gonzales, "*P*-complete approximation problem," *J. ACM*, vol. 23, no. 3, July 1976, pp. 555-565.
- [191]S. Sastry and A. Parker, "The Complexity of Two-Dimensional Compaction of VLSI Layouts," *Proc. International Conference on Circuits and Computers*, New York, 1982, pp. 402-406.
- [192]R. W. Scheifler and J. Gettys, "The X Window System," *ACM Transactions on Graphics*, Vol. 5, No. 2, 1986, pp. 79-109.
- [193]A. T. Schreiner and H. G. Friedman, Introduction to Compiler Construction with UNIX, (Englewood Cliffs; Prentice Hall, 1985), pp. 21-81.
- [194]D. G. Schweikert and B. W. Kernighan, "A Proper Model for the Partitioning of Electrical Circuits," *Proc. 9th Annual Design Automation Workshop*, 1972, pp. 57-62.
- [195]C. Sechen, "Chip-Planning, Placement, and Global Routing of Macro/Custom Cell Integrated Circuits Using Simulated Annealing." *Proc. 25th Design Automation Conference*, 1988, pp. 73-80.
- [196]C. Sechen, *VLSI Placement and Global Routing Using Simulated Annealing*, Kluwer Academic Publishers, 1988.
- [197]C. Sechen and D. Chen, "An Improved Objective Function for Mincut Circuit Partitioning." *Proc. IEEE International Conference on Computer-Aided Design*, 1988, pp. 502-505.
-

- [198]C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *Proc. 1984 Custom Integrated Circuits Conference*, Rochester, New York, May 1984.
- [199]C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *IEEE J. of Solid-State Circuits*, Vol. 20 No. 2, 1985, pp. 432-439.
- [200]C. Sechen, D. Braun, and A. Sangiovanni-Vincentelli. "ThunderBird: A Complete Standard Cell Layout Package." *IEEE J. of Solid-State Circuits* Vol. 23 No. 2, 1985, pp. 410-420.
- [201]C. Sechen and K. W. Lee, "An Improved Simulated Annealing Algorithm for Row-Based Placement," *Proc. of ICCAD*, 1987, pp. 478-481.
- [202]M. Servit, "Heuristic Algorithms for Rectilinear Steiner Trees," *Digital Process*, Vol. 7, No. 1, 1981, pp. 21-31.
- [203]L. Sha and R. Dutton, "An Analytical Algorithm For Placement of Arbitrarily Sized Rectangular Blocks," *Proc. 22nd Design Automation Conference*, 1985, pp. 602-608.
- [204]L. Sha and T. Blank, "ATLAS - A Technique for Layout using Analytic Shapes," *Proc. Intl. Conf. on Computed-Aided Design*, 1987, pp. 84-87.
- [205]K. Shahookar and P. Mazumder, "A Genetic Approach to Standard Cell Placement Using Meta-Genetic Parameter Optimization," *IEEE Trans. on Computer-Aided Design*, Vol. 9, No. 5, May 1990, pp. 500-513.
- [206]N. Shahmehri, M. Kamkar, and P. Fritzon, "Semi-automatic Bug Localization in Software Maintenance," *Proc. IEEE Conference of Software Maintenance*, 1990, pp. 30-36.
- [207]H. Shin and A. Sangiovanni-Vincentelli, "A Detailed Router Based on Incremental Routing Modifications: Mighty," *IEEE Trans. Computer-Aided Design* Vol. 6, No. 6, 1987, pp. 942-955.
-

- [208]E. Shragowitz, J. Lee, and S. Sahni, "Placer-Router for 'Sea of Gates' Design Style," *Proc. International Conference on Computer Design*, October 1987, pp. 330-335.
- [209]P. Siarry, L. Bergonzi, and G. Dreyfus, "Thermodynamic Optimization of Block Placement," *IEEE Trans. on Computer-Aided Design of ICs and Systems*, Vol. 6, No. 2, 1987, pp. 211-221.
- [210]G. Sigl, K. Doll, and F. M. Johannes, "Analytical Placement: A Linear or a Quadratic Objective Function?" *Proc. Design Automation Conference*, pp. 427-432.
- [211]A. Srinivasan, "An Algorithm for Performance-Driven Initial Placement of Small-Cell ICs," *Proc. Design Automation Conference*, June 1991, 636-639.
- [212]A. Srinivasan, K. Chaudhary, and E. Kuh, "RITUAL: A Performance Driven Placement Algorithm for Small Cell ICs," *Proc. Int. Conf. on Computed-Aided Design*, 1991, pp. 48-51.
- [213]L. Steinberg, "The Backboard Wiring Problem: A Placement Algorithm," *SIAM Review*, Vol. 3, No. 1, 1961, pp. 37-50.
- [214]P. Suaris and G. Kedem, "Quadrissection: A New Approach to Standard Cell Layout," *Proc. Intl. Conf. on Computed-Aided Design*, 1987, pp. 474-477.
- [215]P. Suaris and G. Kedem, "An Algorithm for Quadrissection and its Application to Standard Cell Placement," *IEEE Trans. on CAS*, Vol. 35, No. 3, March 1988, pp. 294-303.
- [216]P. Suaris and G. Kedem, "A Quadrissection-based Combined Place and Route Scheme for Standard Cells," *IEEE Trans. on CAD*, Vol. 8, No. 3, March 1989, pp. 234-244.
- [217]S. Sutanthavibul, and E. Shragowitz, "An Adaptive Timing-Driven Layout for High Speed VLSI," *Proc. Design Automation*, June 1990, pp. 90-95.
-

- [218] S. Sutanthavibul, and E. Shragowitz, "Dynamic Prediction of Critical Paths and Nets for Constructive Timing-Driven Placement," *Proc. Design Automation*, June 1991, pp. 632-635.
- [219] W. Swartz, H. Khan, D. A. Thomas, C. R. Giuffre, M. deWit, T. Pavey, C. McIntosh, and W. H. Banzhaf, "CMOS RAM, ROM, and PLA Generators for ASIC Applications," *Proc. Custom Integrated Circuits Conference*, 1986, pp. 334-338.
- [220] W. Swartz and C. Sechen, "New Algorithms for the Placement and Routing of MacroCells," *Proc. Int. Conf. on Computed-Aided Design*, 1990, pp. 336- 339.
- [221] T. Tanaka, T. Kobayashi, and O. Karatsu, "HARP: Fortran to Silicon," *IEEE Trans. Computer-Aided Design*, Vol. 8, No. 6, June, 1989, pp. 649-660.
- [222] R. E. Tarjan, Data Structures and Network Algorithms, (Philadelphia: Society for Industrial and Applied Mathematics, 1983), pp. 2-6.
- [223] K. O. ten Bosch, P. Bingley, and P. van der Wolf, "Design Flow Management in the NELSI CAD Framework," *Proc. Design Automation Conference*, 1991, pp. 711-716.
- [224] M. Terai, K. Takahashi, and K. Sato, "A New Min-Cut Placement Algorithm for Timing Assurance Layout Design Meeting Net Length Constraint," *Proc. Design Automation Conference*, June 1990, pp. 96-102.
- [225] H. F. Trickey, "A High-Level Hardware Compiler," *IEEE Trans. Computer-Aided Design*, Vol. CAD-6, No. 2, March, 1987, pp. 259-269.
- [226] J. Trnka, R. Hedman, G. Koehler, and K. Ladin, "A Device Level Auto Place and Wire Methodology for Analog and Digital Masterslice," *Proc. ISSCC*, 1988, pp. 260-261.
- [227] R. Tsay, E. Kuh, and C. Hsu, "PROUD: A Fast Sea-Of-Gates Placement Algorithm," *Proc. 25th Design Automation Conference*, 1988, pp. 318-323.
-

- [228]R. Tsay and J. Koehl, "An Analytic Net Weighting Approach for Performance Optimization in Circuit Placement," *Proc. Design Automation Conference*, June 1991, pp. 620-625.
- [229]M. Upton, K. Samii, and S. Sugiyama, "Integrated Placement for Mixed Macro Cell and Standard Cell Designs," *Proc. Design Automation Conference*, 1990, pp. 32-35.
- [230]P. van den Hammer and M. A. Treffers, "A DataFlow Based Architecture for CAD Frameworks," *Proc. ICCAD*, 1990, pp. 482-485.
- [231] L. P. van Ginneken and R. H. Otten, "Global Wiring for Custom Layout Design," *Proc. International Symposium on Circuits and Systems*, June 1985, pp. 207-208.
- [232]A. Vannelli, "Interior Point Method for Solving the Global Routing Problem," *Proc. IEEE 1989 Custom Integrated Circuits Conference*, May 1989, paper 3.4.
- [233]A. Vannelli, "An adaptation of the interior point method for solving the global routing problem," *IEEE Trans. on Computer-Aided Design*, Vol 10. No. 2, Feb. 1991, pp. 193-203.
- [234]R. Weier, "TimberWolfAR: An Arbitrary Design Rule Multi-Layer Area Router", paper 2.2 Vol. 1, *Proc. International Workshop on Layout Synthesis*, May 18-21, 1992. MCNC Research Triangle Park, N.C. , pp. 45-46.
- [235]G. M. Weinberg, The Psychology of Computer Programming, (New York: Van Nostrand Reinhold, 1971).
- [236]N. Weste, "Virtual Grid Symbolic Layout", *Proc. 18th Design Automation Conference*, June 1981, pp. 225-233.
- [237]N. Wirth, "Program Development by Step-Wise Refinement," *Communications of the ACM*, Vol. 14, No. 4, 1971, pp. 221-227.
- [238]D.F. Wong and C.L. Liu, "A New Algorithm for Floorplan Design," *Proc. 23rd Design Automation Conference*, 1986, pp. 101-105.
-

- [239]D.F. Wong and C.L. Liu, "Floorplan Design for Rectangular and L-Shaped Modules," *Proc. Intl. Conf. on Computed-Aided Design*, 1987, 520-523.
- [240]G. Wong, "Analog Integrated Circuit Placement Optimization by Simulated Annealing," Master's thesis MIT, 1985.
- [241]O. Yasushi, T. Ishii, *et al.*, "Efficient Placement Algorithms Optimizing Delay for High-Speed ECL Masterslice LSI's." *Proc. 23rd Design Automation Conference*, 1986, pp. 404-410.
- [242]J. Y. Yen, "Finding the K Shortest Loopless Paths in a Network," *Management Science*, Vol. 17, July 1971, pp. 712-716.
- [243]H. Youssef, "Timing Issues in Cell Based VLSI Design," Ph. D. Dissertation, Computer Science Department, University of Minnesota, January, 1990.
-